REMARKS

Claims 1 - 38 are pending in the present application.

In section 2 of the Office Action, claims 1 – 38 are rejected under 35 U.S.C. 102(e) as being unpatentable over U.S. Patent No. 6,378,123 to Dupenloup (hereinafter "the Dupenloup patent"). The present application contains four independent claims, namely claims 1, 11, 21 and 30. Applicants are amending claims 1, 11, 21 and 30 to recite a feature that is neither disclosed nor suggested by the Dupenloup patent.

Claim 1 provides an automated method for designing an integrated circuit (IC) design-specific cell. The method includes, *inter alia*, altering a transistor-level representation of a design-specific cell to meet a design specification.

The Dupenloup patent discloses a system for analyzing a circuit design at the RTL level (col. 6, lines 30 – 31). At the RTL level of abstraction, an IC design is specified by describing operations that are performed on data as it flows between circuit inputs, outputs, and clocked registers (col. 1, lines 24 – 28). The IC design, as expressed by RTL code, is then synthesized to generate a gate-level description, or a netlist (col. 1, lines 30 – 31). Synthesis is the step taken to translate the architectural and functional descriptions of the design, represented by RTL code, to a lower level of representation of the design such as logic-level and gate-level descriptions (col. 1, lines 33 – 36).

The Dupenloup patent also explains that an integrated circuit chip comprises cells and connections between the cells (col. 1, lines46 – 47) A cell is a group of one or more circuit elements such as transistors, capacitors, and other basic circuit elements grouped to perform a function. The Dupenloup patent further states, at col. 78, line 65 – col. 79, line 3:

> A chip may contain several million transistors. Layout of the entire circuit cannot be handled due to the limitation of memory space as well as the computation power available. Therefore it is normally partitioned by

> grouping the components into blocks such as subcircuits and modules. (Emphasis added).

Thus, the Dupenloup patent mentions transistors, yet emphasizes that the layout is conducted at a block level. Moreover, the Dupenloup patent does not mention or suggest that the technique described therein alters a transistor-level representation of a cell in a circuit.

Hence, the Dupenloup patent discloses:

(a) analyzing a circuit design at the RTL level;

(b) synthesizing a design to a gate level or logic level;

(c) that a cell is a group of circuit element, such as transistors;

(d) that the layout of an entire circuit cannot be handled; and

(e) that the layout of a chip is normally partitioned by grouping components into blocks, and

does not mention or suggest:

(f) altering a transistor-level representation of a cell in a circuit.

Accordingly, Applicants submit that the Dupenloup patent does not disclose **altering a transistor-level representation** of a design-specific cell to meet a design specification, as recited in claim 1. Accordingly, Applicants also submit that the Dupenloup patent does not anticipate claim 1.

Independent claims 11, 21 and 30 each includes a recital similar to that of claim 1, as described above. Thus, Applicants further submit that claims 11, 21 and 30 are also novel over the Dupenloup patent.

Claims 2 – 10, 31 and 35 depend from claim 1. Claims 12 – 20, 32 and 36 depend from claim 11. Claims 22 – 29, 33 and 37 depend from claim 21. Claims 34 and 38 depends from claim 30. By virtue of these dependencies, claims 2 – 10, 12 – 20, 22 – 29, and 31 – 38 are also novel over the Dupenloup patent.

Applicants respectfully request reconsideration and withdrawal of the section 102(e) rejection of claims 1 – 38.

As mentioned above, Applicants are amending claims 1, 11, 21 and 30 to recite a feature that is neither disclosed nor suggested by the Dupenloup patent.. Applicants are also amending various claims to do one or more of (a) provide consistent usage of terms, (b) avoid a recital of "means for", (c) correct a dependency, and (d) improve grammar. None of the amendments is intended to narrow the scope of any term of any of the claims, and therefore, the doctrine of equivalents should be available for all of the terms of all of the claims.

In view of the foregoing, Applicants respectfully submit that all claims presented in this application patentably distinguish over the prior art. Accordingly, Applicants respectfully request favorable consideration and that this application be passed to allowance.

Respectfully submitted,

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Date

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